PATENT COOPERATION TREATY

From the:
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

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PCT

WRITTEN OPINION
(PCT Rule 66)

Date of mailing *(day/month/year)*	18 MAR 2004
Applicant's or agent's file reference	SJS:FP18145
REPLY DUE	within **TWO MONTHS** from the above date of mailing

International Application No.	International Filing Date *(day/month/year)*	Priority Date *(day/month/year)*
PCT/AU2003/000994	6 August 2003	7 August 2002

International Patent Classification (IPC) or both national classification and IPC
Int. Cl. [7] G06F 9/50, 12/00

Applicant
MMAGIX TECHNOLOGY LIMITED et al

1. This written opinion is the **first** drawn by this International Preliminary Examining Authority.
2. This opinion contains indications relating to the following items:.

I	[X]	Basis of the opinion
II	[ ]	Priority
III	[ ]	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
IV	[X]	Lack of unity of invention
V	[X]	Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
VI	[ ]	Certain documents cited
VII	[ ]	Certain defects in the international application
VIII	[ ]	Certain observations on the international application

3. The **FINAL DATE** by which the international preliminary examination report must be established according to Rule 69.2 is:
7 December 2004

4. The applicant is hereby **invited to reply** to this opinion.

When? See the **Reply Due** date indicated above. However, the Australian Patent Office will not establish the Report before the earlier of (i) a response being filed, or (ii) one month before the **Final Date** by which the international preliminary examination report must be established. The Report will take into account any response (including amendments) filed before the Report is established.
If no response is filed by 1 month before the Final Date, the international preliminary examination report will be established on the basis of this opinion.
Applicants wishing to have the benefit of a further opinion (if needed) before the report is established should ensure that a response is filed at least **3 months before the Final Date** by which the international preliminary examination report must be established.

How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3.
For the form and the language of the amendments, see Rules 66.8 and 66.9.

Also For an additional opportunity to submit amendments, see Rule 66.4.
For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4*bis*.
For an informal communication with the examiner, see Rule 66.6.

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WRITTEN OPINION

International application No.
PCT/AU2003/000994

I. Basis of the opinion

1. With regard to the elements of the international application:*

[X] the international application as originally filed.

[ ] the description, pages , as originally filed,
pages , filed with the demand,
pages , received on with the letter of

[ ] the claims, pages , as originally filed,
pages , as amended under Article 19,
pages , filed with the demand,
pages , received on with the letter of

[ ] the drawings, pages , as originally filed,
pages , filed with the demand,
pages , received on with the letter of

[ ] the sequence listing part of the description:
pages , as originally filed
pages , filed with the demand
pages , received on with the letter of

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language which is:

[ ] the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

[ ] the language of publication of the international application (under Rule 48.3(b)).

[ ] the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the written opinion was drawn on the basis of the sequence listing:

[ ] contained in the international application in printed form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readable form.

[ ] The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. [ ] The amendments have resulted in the cancellation of:

[ ] the description, pages

[ ] the claims, Nos.

[ ] the drawings, sheets/fig.

5. [ ] This opinion has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed"*

WRITTEN OPINION

International application No.
PCT/AU2003/000994

IV. Lack of unity of invention

1. In response to the invitation (Form PCT/IPEA/405) to restrict or pay additional fees the applicant has:

- [ ] restricted the claims.
- [ ] paid additional fees.
- [ ] paid additional fees under protest.
- [ ] neither restricted nor paid additional fees.

2. This Authority found that the requirement of unity of invention is not complied with for the following reasons and chose, according to Rule 68.1, not to invite the applicant to restrict or pay additional fees:

The international application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept. In coming to this conclusion this Authority has found that there are different inventions as follows:

1. Claims 1,122,144,621,643,1120,1142 and any relevant dependent claim(s).
Method, system or apparatus which involves the delegating of execution-instructions between processing resources via an instruction execution router.

2. Claim 17 and any relevant dependent claim(s).
Apparatus comprising memory that includes an instruction unit which memory may be accessed simultaneously by processing resources wherein the processing resources and memory are on the same die.

3. Claim 36 and and any relevant dependent claim(s).
Apparatus comprising a memory cache disposed in communication with an instruction determination unit and an instruction execution unit wherein both units store values into the memory within a single cycle.

4. Claim 55 and any relevant dependent claim(s).
Apparatus comprising an arbitration unit that includes a priority bit comparator wherein the unit is communicatively disposed with processing resources.

5. Claim 75 and any relevant dependent claim(s).
A medium whose execution-instruction signals involve a processing resource identifier that identifies the origin of an execution signal and an operation code that identifies a target processing resource

6. Claim 85 and any relevant dependent claim(s).
Processor with an integer processing unit, math processing unit and a router that interfaces between the units wherein the router is adapted to route the request from the integer processing unit to the math processing unit.

7. Claim 101 and any relevant dependent claim(s).
Processor with processing units and a cache unit wherein each of the processing units is configured to sleep after sending an access request to the cache unit.

8. Claim 111 and any relevant dependent claim(s).
Processor with internal and external cache units wherein the internal and external cache units is divided into instruction and data areas and the data areas are further subdivided into local and global areas.

NOTE: See Supplemental Box II

3. Consequently, the following parts of the international application were the subject of international preliminary examination in establishing this report:

- [ ] all parts.
- [X] the parts relating to claims Nos. 1-16, 101-110, 121-172, 620-671 and 1119-1170

WRITTEN OPINION

International application No.
PCT/AU2003/000994

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	121,620,1119	YES
	Claims	1-16,101-110,122-172,621-671,1120-1170	NO
Inventive step (IS)	Claims	121,620,1119	YES
	Claims	1-16,101-110,122,172,621-671,1120-1170	NO
Industrial applicability (IA)	Claims	1-16,101-110,121-172,620-671,1119-1170	YES
	Claims		NO

2. Citations and explanations

D1 = US 5522083 D2 = EP 794492 D3 = US 5159689 D4 = US 4346435
D5 = EP 385136 D6 = US 6035374 D7 = US 5860158 D8 = US 5210828

NOVELTY (N): Claims 1-16,101-110,122-172,621-671,1120-1170

First invention (claims 1, 122, 144, 621, 643, 1120, 1142 and dependent claims)

Claim 1 and dependent claims:

Citation US 5522083 is relevant.

The abstract teaches that the entire image processor (apparatus) including individual processors (processing resources), the crossbar switch (router) and memories is contained on a single silicon chip.

The following applies when the image processor (apparatus) is in a SIMD mode (column 63 lines 18 to 54):

- Only one of several processors becoming a primary processor (column 36 line 25) which performs instruction fetch on behalf of the rest of the other processors (which becomes secondary processors - column 36 lines 12 to 16).
- the instruction is fetched when the main processor accesses via an instruction port the instruction from the instruction memory and supplies (delegates) via the switch matrix (router) to the instruction port of secondary processors the fetched instruction.

In view of such disclosures, the arrangement in the claims cannot be considered novel.

Claims 122,621,1120 and dependent claims:

The only difference between claim 1 and claims 122, 621 and 1120 is that the latter claims specify that the memory itself includes "instruction execution logic". It is uncertain as to the nature of this "instruction execution logic" and due to a lack of working interrelationship, it is uncertain if this logic within memory is essential. In any case, column 17 line 1 to column 20 line 11 shows that each crosspoint of the crossbar switch matrix (router) has logic circuitry for accessing memory. These logic circuitries could be considered as the "instruction execution logic" of the crossbar switch. As the crossbar switch and memory are linked and are furthermore found on the same die, then it could be said that the memory itself includes the "instruction execution logic" ie the crossbar switch forms part of the memory.

In view of such disclosures, the arrangement in the claims cannot be considered novel.

NOTE: Refer to Supplemental Box I.

Supplemental Box I

Continuation of Box V.2. Citations and explanations.

Claim 1 and dependent claims:

Citation US 5159689 is relevant.

- The citation's processor includes three functional blocks with individual logic circuits (column 9 lines 48 to 49, figure 16, figure 24). The individual logic circuits of the blocks are processing resources.
- One of these circuits delegates tasks to another one of the circuits as required (column 18 lines 15 to 48).
- The tasks signals are sent to another via control gate circuit (router) (column 18 lines 42 to 48, column 19 line 61).

The disclosures in column 21 line 39 to column 22 line 43, column 23 line 67 to column 34, figure 29 and 35 in particular are also relevant. In view of such disclosures, the arrangement in the claims cannot be considered novel.

The disclosures in citations US 4346435 and EP 385136, being similar to those in citation US 5159689, also anticipate the claimed arrangement.

Claims 144,643,1142 and dependent claims:

Citation EP 794492 is relevant.

In the citation, a system/host CPU (1st processing resource) delegates to a slave processor when the system CPU is unable to execute the codes (column 3 line 49 to column 4 line 27). The slave processor then sleeps.

In view of such disclosures, the arrangement in the claims cannot be considered novel.

Second invention (claim 101 and dependent claims)

US 6035374 is relevant.

It features the following:

- several processors one of which is designated primary **unit** (column 7 lines 36 to 64, figure 3). The processor units (virtual) are effectively the processing units of the claims.
- Each processor unit is capable of executing independently (column 7 lines 11 to 15).
- All of the processors share a cache memory 105 (figure 1).
- Wherein after accessing a cache, a processor unit may go into a nap or a longer sleep mode (column 8 lines 8 to 34, column 16 lines 9 to 17).

In view of such disclosures, the arrangement in the claims cannot be considered novel.

INVENTIVE STEP (IS): Claims 1-16,101-110,122-172,621-671,1120-1170

As above.

Supplemental Box II

Continuation of BOX IV.2.

9. Claims 121,620,1119 and any relevant dependent claim(s).
Method, system or apparatus that involves setting processing resources waiting on shared and locked memory being accessed by other processing resources to sleep until the memory is unlocked.

10. Claims 173,672,1171 and any relevant dependent claim(s).
Method, system or apparatus that involves determining a priority dead-lock-avoidance value wherein the value is used to select among multiple requests with equal priority

11. Claims 211,710,1209 and any relevant dependent claim(s).
Method, system or apparatus that involves preparing a response into a result register wherein the response includes a requesting processing resource identifier and presenting the response to all processing resources.

12. Claims 244,743,1242 and any relevant dependent claim(s).
Method, system or apparatus that involves waking a requesting processing resource if a requesting processing resource identifier identifies the instant processing resource and waking a processing resource if a processing resource is waiting to be unlocked.

13. Claims 278,777,1276 and any relevant dependent claim(s).
Method, system or apparatus that involves comparing a target memory address with register values wherein register values are used to establish a data type of the target memory address for subsequent storage in an apportioned region of cache memory.

14. Claims 319,818,1317 and any relevant dependent claim(s).
Method, system or apparatus that involves a literal constant and a literal prefix relating to a reduced size execution of execution-instructions.

15. Claims 360,859,1358 and any relevant dependent claim(s).
Method, system or apparatus that involves replacing odd address value in an instruction register with an even address found in a binding name table.

16. Claims 118,395,617,894,1116,1393 and any relevant dependent claim(s).
Method, system or apparatus that involves a status register as well as addressing a register specified by a register address or cycle flags.

17. Claims 431,930,1429 and any relevant dependent claim(s).
Method, system or apparatus that involves requesting that a requesting processing resource sleep until it is unlocked if a target memory is locked

18. Claims 468,967,1466 and any relevant dependent claim(s).
Method, system or apparatus that involves determining value types by using a hash function as well as updating value types in a primary cache memory of a processing resource to a secondary cache memory for each type value, if each value type in a primary cache has not been updated to a secondary cache memories.

19. Claims 508,509,546,1008,1045,1507,1544 and any relevant dependent claim(s).
Method, system or apparatus that involves an event variable and the waking of a processing resource from sleep that is waiting on an event if the event value is set not to sleep.

20. Claims 581,1080,1579 and any relevant dependent claim(s).
Method, system or apparatus that involves wait-on semaphore instruction, signal-on semaphore instruction and operating system trap-call.

Since the abovementioned groups of claims do not appear to share any technical features, a "technical relationship" between the inventions, as defined in PCT rule 13.2 does not exist. Accordingly the international application does not relate to one invention or to a single inventive concept, a priori.